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10/701,526	11/06/2003	Bruce B. Doris	FIS920030246	2507

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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,526	DORIS ET AL.	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The disclosure has support for both n-channel and p-channel transistors having a first plurality of n-channel field effect transistors having spacing between adjacent n-channel field effect transistors that fall within a first defined spacing range; a second plurality of n-channel field effect transistors having spacing between adjacent n-channel field effect transistors that fall within a second defined spacing range separately and a first plurality of p-channel field effect transistors having spacing between adjacent p-channel field effect transistors that fall within a third defined spacing range; a second plurality of p-channel field effect transistors having spacing between adjacent p-channel field effect transistors that fall within a fourth defined spacing range; a first tensile layer having a first tensile layer thickness and being configured to impart a first determined tensile stress to the first plurality of n-channel field effect transistors; a second tensile layer having a second tensile layer thickness and being configured to impart a

second determined tensile stress to the second plurality of n-channel field effect transistors; a first compressive layer having a first compressive layer thickness and being configured to impart a first determined compressive stress to the first plurality of p-channel field effect transistors; and a second compressive layer having a second compressive layer thickness and being configured to impart a second determined compressive stress to the second plurality of p-channel field effect transistors. But the disclosure has no support for the both n-channel and p-channel transistors put together on the same substrate as recited in claim 11.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1, 20 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Morin et al., US patent application publication No. US 2004/0135234.

Regarding claim 1, Morin teaches a semiconductor structure (fig. 2) formed on a substrate (NMOS and PMOS transistors inherently are formed on a substrate) comprising: a plurality of field effect transistors (NMOS and PMOS transistors of fig. 3) having a first portion (NMOS) of field effect transistors (FETS) and a second portion (PMOS) of field effect transistors; a first stress layer

(σ_1) having a first thickness and being configured to impart a first determined stress to the first portion of the plurality of field effect transistors (PMOS region); and a second stress layer (σ_2) having a second thickness and being configured to impart a second determined stress to the second portion of the plurality of field effect transistors (NMOS region).

Regarding claim 20, Morin teaches (fig. 3) a process of forming a semiconductor structure, comprising: forming a plurality of field effect transistors on a semiconductor substrate (NMOS and PMOS transistors inherently are formed on a substrate) (fig. 3), the plurality of field effect transistors including a first portion of field effect transistors (PMOS) and a second portion of field effect transistors (NMOS); depositing a first stress layer (SiN2) having a first thickness and being configured to impart a first determined stress to the first portion of the plurality of field effect transistors; and depositing a second stress layer (SiN1 and SiN2) having a second thickness and being configured to impart a second determined stress to the second portion of the plurality of field effect transistors.

Regarding claim 23, Morin teaches (fig. 3) a semiconductor circuit comprising a substrate (NMOS and PMOS transistors inherently are formed on a substrate); a plurality of field effect transistors (NMOS and PMOS) formed on the substrate, the plurality of field effect transistors including a first portion of field effect transistors and a second position of filed effect transistors; a first stress layer (SiN2) having a first thickness and being configured to impart a first determined stress to the first portion (NMOS) of the plurality of field effect transistors; and a second stress layer (SiN1 and SiN2) having a second

thickness and being configured to impart a second determined stress to the second portion of the plurality of field effect transistors (refer also to paragraph [0031] and [0034]).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morin.

Regarding claim 21, Morin teaches substantially the entire claimed structure of claim 20 above except explicitly stating that removing portions of the first stress layer from areas of the semiconductor that would not experience performance enhancement due to the first determined stress; and removing portions of the second stress layer from areas of the semiconductor that would not experience performance enhancement due to the second determined stress.

However Morin teaches forming SiN1 layer on the PMOS region first and forming SiN2 layer on both the PMOS and NMOS regions. The process above entails removing portion of the SiN1 from the NMOS region.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made removing portions of the first stress layer and

the second stress layer as claimed in order to enhance the performance of the NMOS and PMOS field effect transistors.

Regarding claim 22, Morin teaches substantially the entire claimed structure of claim 20 above including the first thickness (SiN2) is less than the second thickness (SiN1+SiN2).

7. Claims 2-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morin in view of Tobben et al. US patent No. 6,235,574.

Regarding claims 2, 3 and 24-25, Morin teaches substantially the entire claimed structure of claims 1 and 23 above except explicitly stating that the first portion of the plurality of field effect transistors have spacings between adjacent field effect transistors that fall within a first defined spacing range; and the second portion of the plurality of field effect transistors have spacings between adjacent field effect transistors that fall within a second defined spacing range, where the first defined spacing range is less than the second defined spacing range.

Tobben teaches (figs. 1-6) the formation of a plurality of field effect transistors where the field effect transistors (the FETS formed in region 100A) have spacings between adjacent field effect transistors that fall within a first defined spacing range; and the second portion of the plurality of field effect transistors (the FETS formed in region 100B) have spacings between adjacent field effect transistors that fall within a second defined spacing range, where the first defined spacing range is less than the second defined spacing range.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form field effect transistors as taught by Tobben in the structure of Morin in order to form a high performance DRAM.

Furthermore Morin teaches the first thickness (the thickness of SiN2 is less than the combined thickness of SiN1 plus SiN2) is less than the second thickness (refer to fig. 3).

Regarding claim 4, Morin teaches substantially the entire claimed structure of claim 1 above including the first thickness does not pose a substantial risk of void formation in the first stress layer. No voids are formed in the structure of Morin.

Regarding claim 5, Morin teaches substantially the entire claimed structure of claim 1 above including the first determined stress enhances performance of the first portion of the plurality of field effect transistors, without materially degrading performance of any of the plurality of FETs that are not in the first portion; and the second determined stress enhances performance of the second portion of the plurality of field effect transistors, without materially degrading performance of any of the plurality of FETs that are not in the second portion (refer to paragraph [0031] to [0035]).

Regarding claims 6-8, Morin teaches substantially the entire claimed structure of claim 1 above including the first portion of the plurality of field effect transistors is comprised of n-channel field effect transistors (NMOS); the first determined stress is a tensile stress (refer to paragraph [0034], positive stress is associated with tensile stress); the second portion of the plurality of field effect

transistors is comprised of p-channel field effect transistors (PMOS); and the second determined stress is a compressive stress (refer to paragraph [0031] negative stress is also known as compressive stress) .

The limitations that the first stress layer is formed by a chemical vapor deposition process using a temperature of about 480° C, a pressure of about 6.25 Torr, a spacing between the semiconductor structure and CVD electrode of about 490 mils, a flow of about 300 sccm of 2% dilate SiH4 gas, about 15 sccm NH3 gas and about 1060 scan NZ gas using RIF power of about 340 watts and the second stress layer is formed by a chemical vapor deposition process using a temperature of about 480°, a pressure of about 5.75 Torr, a spacing between the semiconductor structure and CVD electrode of about 395 mils, a flow of about 3000 scan of 2% dilute SiH4 gas, about 15 sccm of NH3 gas and 1060 sccm of NZ gas using RF power of 900 watts are not given patentable weight because it is considered a product-by-process claim. "[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claim 9, Morin teaches substantially the entire claimed structure of claims 1, 4 and 6 above including the first portion of the plurality of field effect transistors is comprised of n-channel field effect transistors; the first

determined stress is a tensile stress (refer to paragraph [0034]); the first defined spacing range is less than the second defined spacing range and the first thickness does not pose a substantial risk of void formation in the first stress layer.

Morin does not teach the second portion of the plurality of field effect transistors is comprised of n-channel field effect transistors; the second determined stress is a tensile stress; the first thickness is less than the second thickness.

Morin establishes in paragraph [0034] that a positive stress that is tensile stress enhances the performance of an NMOS device. Furthermore Tobben shows the formation DRAM structure with a plurality of NMOS and PMOS transistors.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a second portion of the plurality of field effect transistors comprised of n-channel field effect transistors as claimed in the combined structure of Morin and Tobben in order to form a high performance DRAM structure.

Furthermore parameters such as thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the first and second thickness as claimed in order to form a high performance DRAM structure.

Regarding claim 10, Morin teaches (fig. 4) substantially the entire claimed structure of claims 1 and 5 above including the first portion of the plurality of field effect transistors is comprised of p-channel field effect transistors (PMOS); the first determined stress is a compressive stress (refer to paragraph [0031]); the first defined spacing range is less than the second defined spacing range and the first thickness does not pose a substantial risk of void formation in the first stress layer.

Morin does not teach the second portion of the plurality of field effect transistors is comprised of p-channel field effect transistors; the second determined stress is a compressive stress and the first thickness is less than the second thickness.

Morin establishes in paragraph [0031] that a negative stress that is a compressive stress enhances the performance of a PMOS device. Furthermore Tobben shows the formation DRAM structure with a plurality of NMOS and PMOS transistors.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a second portion of the plurality of field effect transistors comprised of p-channel field effect transistors as claimed in the combined structure of Morin and Tobben in order to form a high performance DRAM structure.

Furthermore parameters such as thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the first and second thickness as claimed in order to form a high performance DRAM structure.

Regarding claim 11, the combined structure of Morin and Tobben teaches substantially the entire claimed structure of claims 1, 9 and 10 except explicitly stating that a first plurality of n-channel field effect transistors having spacings between adjacent n-channel field effect transistors that fall within a first defined spacing range; a second plurality of n-channel field effect transistors having spacings between adjacent n-channel field effect transistors that fall within a second defined spacing range; a first plurality of p-channel field effect transistors having spacings between adjacent p-channel field effect transistors that fall within a third defined spacing range; a second plurality of p-channel field effect transistors having spacings between adjacent p-channel field effect transistors that fall within a fourth defined spacing range; a first tensile layer having a first tensile layer thickness and being configured to impart a first determined tensile stress to the first plurality of n-channel field effect transistors; a second tensile layer having a second tensile layer thickness and being configured to impart a second determined tensile stress to the second plurality of n-channel field effect transistors; a first compressive layer having a first compressive layer thickness and being configured to impart a first determined compressive stress to the first plurality of p-channel field effect transistors; and a second compressive layer having a second compressive layer thickness and being configured to impart a

second determined compressive stress to the second plurality of p-channel field effect transistors.

Since the combined structure of Morin and Tobben established that both n-FET and p-FET can be arranged separately as in claims 9 and 10, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form both the n-FET and p-FET as claimed in order to form a high performance DRAM structure.

8. Claims 12-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morin, Tobben and in view of Ngo et al. US patent No. 6,483,154.

Regarding claim 12, Morin teaches substantially the entire claimed structure of claim 11 above except explicitly stating that each of the first tensile layer; second tensile layer; first compressive layer and second compressive layer is deposited on an $Si0_2$ liner.

It is conventional in the art and also taught by Ngo forming $Si0_2$ liner (23) with a spacer structure formed of SiN (24) in the structure of transistor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form oxide liner as taught by Ngo in the structure of Morin in order to improve adhesion between the stress layer and the semiconductor device.

Regarding claim 13, Morin teaches substantially the entire claimed structure of claim 11 above except explicitly stating that the first defined spacing range is less than the second defined spacing range; and the third defined spacing range is less than the fourth defined spacing range.

Parameters such as spacing and thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the spacing of the first defined spacing, second defined spacing range and the third defined spacing as claimed in order to form a high performance DRAM structure.

Regarding claim 14, Morin teaches substantially the entire claimed structure of claim 11 above except explicitly stating the first tensile layer thickness is less than the second tensile layer thickness; and the first compressive layer thickness is less than the second compressive layer thickness.

Parameters such as thickness and spacing in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the first tensile layer, the second tensile layer thickness, the first compressive layer thickness and the second compressive layer thickness as claimed in order to form a high performance DRAM structure.

Regarding claim 15, Morin teaches substantially the entire claimed structure of claims 4 and 11 above including the first tensile layer thickness does not pose a substantial risk of void formation in the first tensile layer; and the first

compressive layer thickness does not pose a substantial risk of void formation in the first compressive layer.

Regarding claim 16, Morin teaches substantially the entire claimed structure of claims 5 and 11 above including the first determined tensile stress enhances electron mobility in the first plurality of n-channel field effect transistors, without materially degrading performance of the first plurality of p-channel field effect transistors and the second plurality of p-channel field effect transistors; and the first determined compressive stress enhances hole mobility in the first plurality of p-channel field effect transistors, without materially degrading performance of the first plurality of n-channel field effect transistors and the second plurality of n-channel field effect transistors.

Regarding claim 17, Morin teaches substantially the entire claimed structure of claim 11 above except explicitly stating that the first tensile layer thickness is proportional to the first determined spacing range; the second tensile layer thickness is proportional to the second determined spacing range; the first compressive layer thickness is proportional to the third determined spacing range; and the second compressive layer thickness is proportional to the fourth determined spacing range.

Parameters such as thickness and spacing in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the first tensile layer, the second

tensile layer thickness, the first compressive layer thickness and the second compressive layer thickness as claimed in order to form a high performance DRAM structure.

Regarding claim 18, Morin teaches substantially the entire claimed structure of claim 11 above including the first tensile layer, second tensile layer, first compressive layer and second compressive layer is a silicon nitride.

Regarding claim 19, Morin teaches substantially the entire claimed structure of claim 11 above except explicitly stating that the first tensile layer and second tensile layer each exhibit a tensile stress of about 600 to 1500 MPa; and the first compressive layer and second compressive layer each exhibit a compressive stress of about -600 to -1500 MPa.

Parameters such as tensile stress value and compressive stress value in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the stress brought about by the first tensile layer, the second tensile layer, the first compressive layer and the second compressive layer as claimed in order to form a high performance DRAM structure.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
November 24, 2004

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